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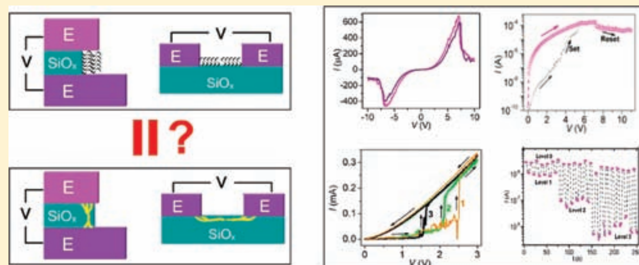
Silicon Oxide: A Non-innocent Surface for Molecular Electronics and Nanoelectronics Studies

Jun Yao,[†] Lin Zhong,[*,‡,§] Douglas Natelson,[*,§,||] and James M. Tour[*,†,⁵]

[†]Applied Physics Program through the Department of Bioengineering, [‡]Department of Computer Science, [§]Department of Electrical and Computer Engineering, [||]Department of Physics and Astronomy, and [⁵]Department of Chemistry, Rice University, 6100 Main Street, Houston, Texas 77005, United States

S Supporting Information

ABSTRACT: Silicon oxide (SiO_x) has been widely used in many electronic systems as a supportive and insulating medium. Here, we demonstrate various electrical phenomena such as resistive switching and related nonlinear conduction, current hysteresis, and negative differential resistance intrinsic to a thin layer of SiO_x. These behaviors can largely mimic numerous electrical phenomena observed in molecules and other nanomaterials, suggesting that substantial caution should be paid when studying conduction in electronic systems with SiO_x as a component. The actual electrical phenomena can be the result of conduction from SiO_x at a post soft-breakdown state and not the presumed molecular or nanomaterial component. These electrical properties and the underlying mechanisms are discussed in detail.



INTRODUCTION

Because of its good insulating properties and mature technologies in fabrication, SiO_x has long been used as a passive and insulating material in electronics. In the construction of typical two-terminal electronic devices, it is frequently used as a supporting substrate for a pair of planar electrodes or as an insulating spacer between a pair of vertical ones. Topologically, this E−SiO_x−E (E denotes electrode) system defines a gap structure across which material of interest can be bridged and electrically measured. Because SiO_x ordinarily contributes negligibly to conduction, the measured electrical properties are solely attributed to the material of interest. Through this approach, electrical transport properties in various molecules and nanomaterials have been investigated.[1−13]

Recently, however, it has been shown that this traditionally passive SiO_x can be readily converted into an electrically active material for resistive-switching memories.[14] The conduction and resistance change occurs through voltage-driven formation and modification of a pathway of silicon (Si) nanocrystals (NCs) embedded in the SiO_x matrix, with SiO_x itself also serving as the source for the formation of Si NCs.[14] This mechanistic picture reveals the intrinsic property of conduction in SiO_x and therefore results in electrode-independent resistive switching in SiO_x.[15] While efforts have been directed toward SiO_x-based memory device fabrication, performance, and mechanism investigation,[14,16] little attention has yet been paid to the implications of this conduction upon other electronic systems that use SiO_x as a device component. In particular, in molecular systems, the spacing between the electrodes tends to be close in order for the molecules, either monolayers or multilayers, to be bridged between the pair of electrodes. Consequently, at modest voltages, high local electric fields are attained in the gap defined by the pair of electrodes. It is then of critical importance to determine whether the measured electrical phenomena are truly the result of molecular conduction or resulting from SiO_x conduction induced by the high electric field.

In this Article, we demonstrate resistive switching in a thin layer of SiO_x (thickness t = 7−100 nm). Depending on the history and sweep mode, we show in detail that one can obtain various nonlinear current−voltage (IV) behaviors, all of which point to the same underlying mechanism. The nonlinear features in the IV curves include current peaks and current hysteresis. At the post soft-breakdown state, we further show that negative differential resistance (NDR) and current hysteresis can be obtained at a lower voltage range (below the resistive-switching voltage range). The electrical phenomena are explained by filamentary conduction in SiO_x. Finally, we show different current hysteretic behaviors from a native silicon oxide surface ($t \approx$ 1.5−3 nm). All these electrical behaviors can largely mimic electrical phenomena observed in molecular and nanoelectronic systems, suggesting substantial caution must be paid when studying conduction in nanoscale systems that use SiO_x as an isolating layer. Starting with a plausible molecular conduction, we then show that this nonlinear conduction is actually from the SiO_x itself and underlies the observed resistive switching. This is done by reproducing the same effect in a bare system without the molecules. Furthermore, by employing a carbon-nanotube network to mimic

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a nanoelectronics study, we show that the initial conduction assists and eventually evolves into SiO_x conduction. The electrical behavior and properties of SiO_x conduction are further discussed, providing potential guides to allow SiO_x conduction to be distinguished from other nanoelectronic behaviors. It should be noted that previous studies[14,16] have mainly focused on the memory properties of SiO_x with layer thicknesses >30 nm, whereas the electrical phenomena discussed here cover the SiO_x thicknesses below 20 nm and down to 2 nm (surface native oxide), therefore closer to molecular dimensions.

■ RESULTS AND DISCUSSION

1. Resistive Switching and Related Nonlinear Conduction. To sandwich molecules between a pair of electrodes, vertical polySi−SiO_x−polySi ($x \approx 2$) stacking structures with diameters of 100 μm were fabricated as illustrated in Figure 1a (see the Supporting Information for details of material preparation). Highly doped polySi layers (ρ < 0.005 Ω cm, thickness = 70 nm) are used here as both top and bottom electrodes to exclude any effects due to motion of metal from the electrodes.[17,18] The two electrodes were spaced by a SiO_x layer with a thickness of 10 nm. By etching away some portion of the SiO_x at the vertical edge in a 10:1 buffered oxide etch (J. T. Baker), a vertical nanogap system was defined, and molecules can be assembled in the nanogap.[7] This structure is similar to other vertical molecular systems in which SiO_x layers were used as insulating and supportive spacers between the top and bottom electrodes.[1−3] 3-Aminopropyltriethoxysilane (APTES) molecular layers at an estimated thickness of 10 nm were then assembled onto the vertical SiO_x surface in the nanogap, following a process described in the literature.[19] All of the electrical characterizations were performed under vacuum (10^{-5} Torr) at room temperature. The successful assembling of the molecules is indicated by the increased conduction as compared to that of a pair of bare electrodes (inset in Figure 1b). During a subsequent series of consecutive voltage sweeps from −12 to +12 V, the current level gradually increased until it reached a certain value after several voltage sweeps; during this process, nonlinear *IV* curves featuring current peaks at ∼±7.5 V were persistently observed (Figure 1b). The nonlinear behavior was approximately symmetric in the negative and positive voltage regions and was very similar to that observed in OPE molecules assembled in metal nanogaps on a SiO_x substrate.[4]

A control experiment in which no APTES molecules were assembled in the polySi−SiO_x−polySi nanogap shows almost the same *IV* curves (Figure 1c). The absence of molecules here indicates that the electrical behavior in the previous system was not intrinsic to the molecules. Instead, it resulted from the soft breakdown of the SiO_x layer at the vertical edge[14] region by the high electric field built in the nanogap. The gradually increased current level upon continuous voltage sweeps (Figure 1b), deviating from the initial conduction (inset in Figure 1b), was a signature of the electroforming[20] process in SiO_x. In fact, similar electrical behaviors were first described in the 1960s in silicon-rich M−SiO_1−M (M denotes metal) sandwiched systems.[21] While different models were proposed for the mechanism,[22] the exclusive use of metal electrodes often led to a mechanistic picture of conduction by metal defects injected from the electrodes.[21] The defective silicon-rich SiO_1 system and the extrinsic metal-filamentary picture have likely contributed to the neglect of the potential conduction from SiO_x in other electronic systems, where x is usually

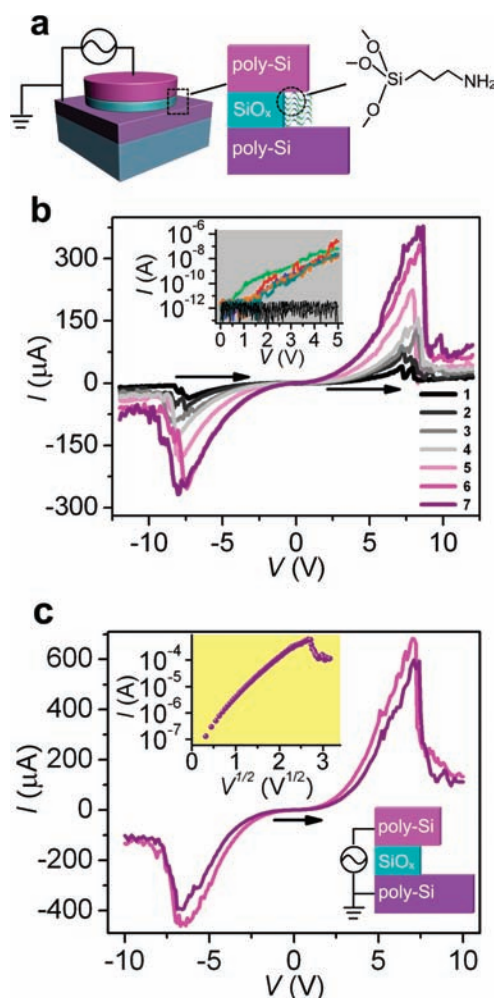

Figure 1. (a) Left panel: Schematic of a vertical polySi−SiO_x−polySi structure (70 nm−10 nm−70 nm) and the electrical-characterization setup. The diameter of the structure is 100 μm. Right panel: An enlarged schematic of the nanogap defined at the vertical edge in which APTES molecular layers are assembled. (b) Consecutive voltage sweeps (−12 V→ 12 V) in a device with APTES molecular layers as shown in (a). The numbers indicate the voltage-sweep orders. Inset shows the conduction before (black curves) and after (color curves) APTES assembling in several devices, with each curve corresponding to one device. (c) *IV* curves (−10 V→ +10 V) in a bare polySi−SiO_x−polySi device without molecules. Note that the device was thermally annealed at 600 °C for 10 min in a reducing environment (Ar/H_2 = 450/150 sccm) prior to the electrical characterization. The top inset shows one of the *IV* curves in the positive bias region in a log(I)−$V^{1/2}$ format. The bottom inset shows a schematic of the vertical edge on which no molecules are assembled.

close to 2 to ensure a good insulating property. Indeed, a recent study[14] revealed details of SiO_x-generated conduction: the voltage-driven electrochemical processes can induce local reduction of SiO_x to form Si nanocrystalline pathways and lead to increased conduction and resistive switching intrinsic to SiO_x. The formation of this localized conduction usually occurs at the SiO_x surface region, which is more defective and therefore easier to induce into a soft breakdown. Here, it was revealed[14] to be at the etched vertical edge of the SiO_x layer. The soft breakdown can be readily induced in SiO_x with various x values (e.g., $1 < x \leq 2$), and the formed electrical behaviors are largely electrode-independent.[15]

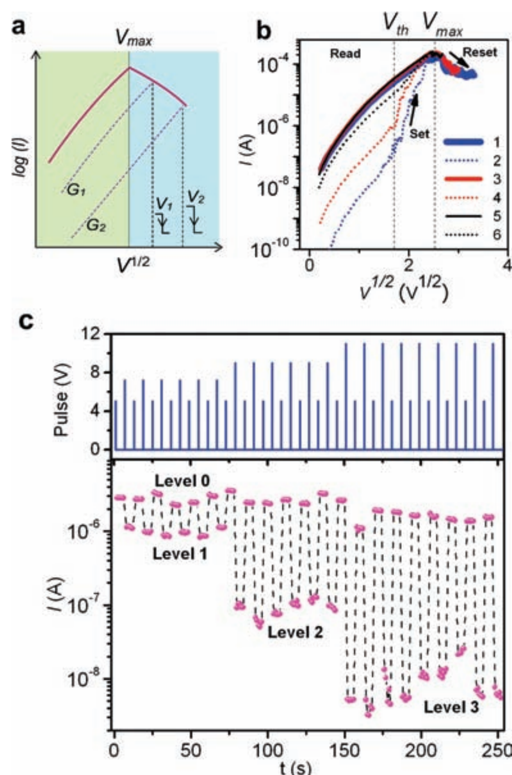

Figure 2. (a) An illustration of the "extrapolation rule" in a $\log(I)-V^{1/2}$ format. (b) Consecutive *IV* curves in a bare vertical polySi−SiO_x−polySi device as illustrated in Figure 1c (lower inset). The numbers indicate the voltage-sweep orders. The solid curves are voltage sweeps from 0 to a value above V_{max}, with blue, red, and black curves corresponding to 0 V → +11 V, 0 V → +9 V, and 0 V → +7 V, respectively. The dashed curves are voltage sweeps from 0 V to a value (+6 V) close to V_{max}. "Read", "set", and "reset" regions are defined by V_{th} and V_{max} as shown in the figure. (c) Top panel: A series of voltage-pulse sets of (+5 V, +7 V), (+5 V, +9 V), and (+5 V, +11 V) working as programming voltages. Bottom panel: Corresponding memory states read by +1 V pulses. Note the programming current is not shown here. The data indicate that a set voltage of +5 V programs the device into the ON state (level 0), whereas reset voltages of different magnitudes (+7 V, +9 V, +11 V) program it into different OFF states (level 1, level 2, and level 3).

In light of the Si-pathway conduction, the nonlinearity in the *IV* curves can be a result of voltage-driven structural changes in the conducting pathways or filaments. The conductance increase and decrease correspond to the construction and destruction of the conducting filaments, respectively. Therefore, the resistance of the SiO_x depends on the history of the voltage sweeps that modified the filaments. For example, if a voltage sweeps above V_{max} (the voltage at the current peak) and then drops fast to 0 V, the resultant resistance of the SiO_x corresponds to the value at this voltage and can be estimated through an "extrapolation rule".[21] This is illustrated in Figure 2a in which the *IV* relationship is presented in a $\log(I)-V^{1/2}$ format, because generally the conduction in SiO_x is dominated by tunneling having the characteristic of $\log(I) \propto V^{1/2}$ (see upper inset in Figure 1c).[21,22] If a voltage sweeps to V_1 and then drops quickly to 0 V, it is expected that the conductance of the SiO_x has been changed to G_1, which can be estimated by drawing an extrapolation line parallel to the initial *IV* curve in the $V < V_{max}$ region (Figure 2a). In a similar way, lower conductance G_2 can be achieved by sweeping to a voltage V_2 ($V_2 > V_1$). This rule is well-demonstrated in

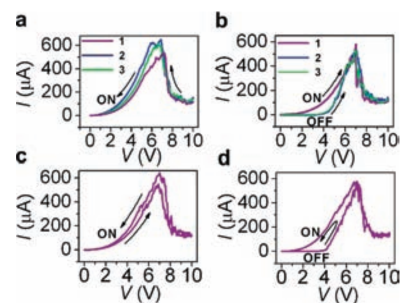

Figure 3. *IV* curves in a vertical polySi−SiO_x−polySi (70 nm−10 nm−70 nm) device by different voltage-sweep modes: (a) single backward sweeps (+10 V → 0 V); (b) single forward sweeps (0 V → +10 V); (c) double sweep (0 V → +10 V → 0 V) starting with an ON state; (d) double sweep (0 V → +10 V → 0 V) starting with an OFF state. The arrows indicate the sweep directions, and the numbers indicate the sweep orders.

the actual *IV* curves in Figure 2b in which each starting conductance (dashed curves) depends on the previous voltage sweep (solid curves) through the "extrapolation rule". The *IV* curves in Figure 2b also define the "read", "set", and "reset" regions that are usually identified in resistive-switching devices.[20] The "reset" region is at $V > V_{max}$, as voltages in this region reset the SiO_x to lower-conductance states. The "set" region begins at a threshold voltage V_{th}, at which the lower conductance suddenly increases and deviates from the original $\log(I) \propto V^{1/2}$ curve in the "read" region. For the above reasons, multilevel nonvolatile resistive memories can be realized by applying voltage pulses of different magnitudes (see Figure 2c).

For the above discussion, depending on the voltage-sweep history and mode, different *IV* behaviors can be observed in SiO_x. For example, for a backward voltage sweep starting from the "reset" region to 0 V, the *IV* curve is always in an ON state in the "read" region as it eventually bypasses the "set" region (Figure 3a). However, for forward voltage sweeps starting from 0 V to a reset voltage, after the first sweep, the subsequent sweeps always have OFF states in the "read" region because each previous sweep ends at the "reset" region (Figure 3b). Similarly, in double-sweep modes, if initially the device is in an ON state, no current hysteresis is produced (Figure 3c). If initially the device is in an OFF state, hysteresis is produced (Figure 3d). This last type of sweep has been frequently used[14−16,23] as characteristic resistive-switching *IV* curves because it indicates both the programming regions and the ON/OFF ratio. Similarly, the electroforming process that converts the pristine SiO_x into a resistive-switching state can also have different *IV* evolutions with respect to different voltage-sweep modes (see Supporting Information Figure S1). The above resistive-switching *IV* curves in SiO_x feature current peaks that resemble those demonstrating NDR effects. However, these effects should not be classified as the specific NDR that results from resonant tunneling.[24] As the underlying cause for resistive switching or conductance change in SiO_x is a voltage-driven modification of the conducting filament, the *IV* curves are sweep-history and sweep-direction dependent (as shown in Figure 3), whereas resonant-tunneling-based NDR does not show that dependency. However, later we will show that SiO_x can still produce similar resonant-tunneling NDR at a lower voltage region.

The current peak in SiO_x conduction can be very sharp (Figure 4a). Consequently, the characteristic resistive-switching

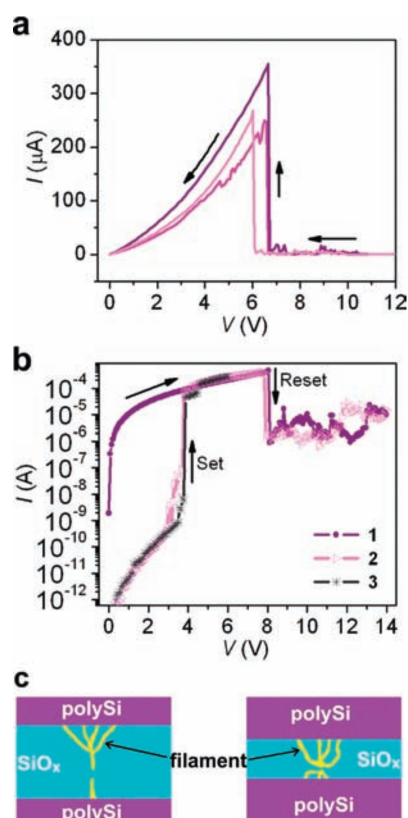

Figure 4. (a) Backward voltage sweeps (+12 V → 0 V) in a vertical polySi−SiO_x−polySi (70 nm−40 nm−70 nm) device, showing steep current peaks. (b) Forward *IV* curves from the same device in (a), showing sharp set and reset threshold voltages. The numbers indicate the sweep order. (c) Illustrations depicting the SiO_x-layer thickness effects on the development of conducting filaments and thus the OFF current. Left panel: An OFF state from a fully developed filament in a comparatively thick SiO_x layer. Right panel: An OFF state from a less effectively developed filament in a thin SiO_x layer. The development of the single filamentary strand in the thick SiO_x layer ensures a low OFF tunneling current, while the lack of this single filamentary strand in the thin SiO_x layer results in an increased cross-section area of tunneling, and thus an increased OFF current.

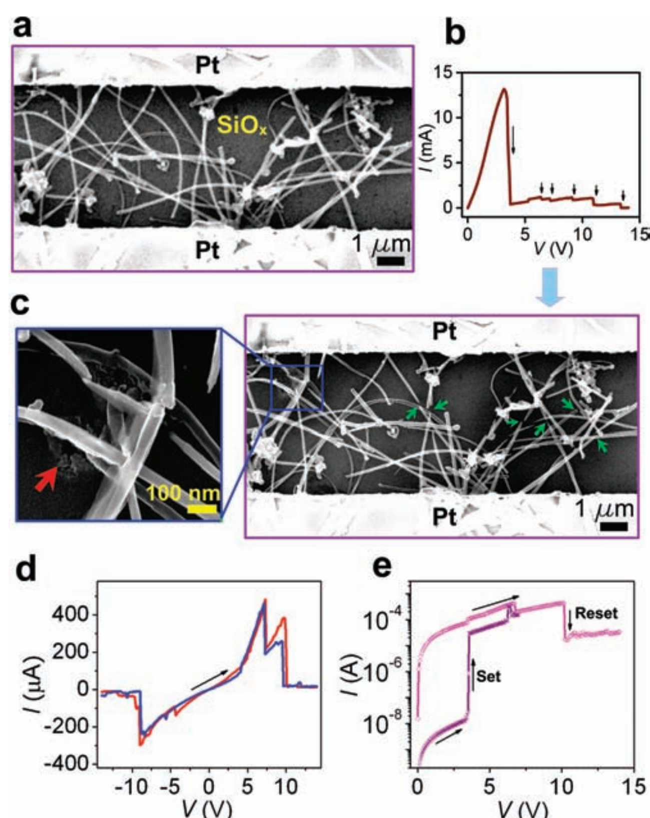

Figure 5. Resistive switching and related nonlinear conduction in a MWCNT network on a Si substrate capped with 200 nm thermally grown SiO_2. (a) A scanning electron microscopy (SEM) image of the random MWCNT network. (b) Initial voltage sweep (0 V → +14 V). The black arrows indicate sudden current drops, or electrical breakdowns in MWCNTs. (c) SEM image of the same MWCNT-network device after the voltage sweep in (b). The green arrows indicate broken regions in different MWCNTs. The inset on the left panel is a higher magnification picture of the MWCNT network. It shows the broken regions of MWCNTs, along with observable damage to the underlying SiO_2 substrate (indicated by the red arrow). (d) *IV* curves featuring current peaks in the same electroformed device. The multiple peaks are likely caused by multiple MWCNT−SiO_x−MWCNT resistive-switching sites. (e) Characteristic resistive-switching *IV* curves in the same device.

IV curves feature sharp set and reset threshold voltages (Figure 4b). As resistive switching in SiO_x is through filamentary conduction, the differences in the *IV* curves can be considered as the consequence of different evolutions in the filament. In the proposed mechanistic picture of an electrochemical redox process of Si⇆SiO_x at the resistive-switching site,[14] it can be understood that the effectiveness of this process, even in a single filament, can commensurately modulate the conductance change. For example, a more effective oxidation process of Si→SiO_x at the resistive-switching site is expected to cause a more abrupt decrease in the OFF conduction. The dynamics of the resistive-switching process, including the degree to which redox switching of Si/SiO_x can be cooperative at multiple sites, may well be affected by internal stress distributions associated with the glassy SiO_x structure.[25] A restricted film thickness is likely to hinder the formation of a single filamentary strand (as illustrated in Figure 4c), resulting in an increased cross-sectional area of tunneling in the OFF state, and thus the increased OFF current. This is consistent with our observation that the average ON/OFF ratios in a thin SiO_x film (10 nm) were typically within 10^3, as compared to ratios exceeding 10^4 in a thicker SiO_x film (40 nm); this is mainly due to the increased current in the OFF states. It also raises the question: At what thickness does SiO_x still demonstrate resistive switching and related nonlinear behavior? Our experiments indicate that similar reproducible electrical phenomena can be induced in SiO_x with thicknesses ranging from 7 to 200 nm, covering a majority of nanogaps defined on SiO_x for molecular and nanoelectronic systems that have been studied.

With the assistance from other conducting pathways, this SiO_x thickness could extend far beyond 200 nm. We used a network of multiwalled carbon nanotubes (MWCNTs) to mimic a random molecular layer or other conducting nanomaterials on a Si substrate capped with 200 nm thermally grown SiO_x ($x = 2$, Silicon Quest International, Inc.) and patterned the network with two electrodes over 5 μm apart (Figure 5a). By sweeping to +14 V, multiple sudden conductance decreases are observed (Figure 5b) as a result of electrical breakdowns in the MWCNTs. This is also visible in the physical breaking of MWCNTs (Figure 5c, indicated by green

arrows). Upon further voltage sweeps, the SiO_x between certain nanogap defined by two broken ends of MWCNT can form soft breakdown and be electroformed to a resistive-switching state. This process is always accompanied by visible morphological change to the SiO_x at the nanogap region (left panel in Figure 5c), which is a signature of the electroforming process in various resistive-switching materials.[14,15,22] Hence, starting with a conduction initially coming from the MWCNT-network, the conduction eventually evolves into reproducible nonlinear behavior and resistive switching coming from SiO_x (Figure 5d,e), with the broken MWCNT network merely serving as effective nanospaced electrodes.

The above MWCNT network offers a vivid example of how conductive molecular layers or nanomaterials can assist the formation of SiO_x conduction; the disruption of molecular layers or nanomaterials, either by local electrical breakdown or by nonuniformity during assembly, helps to build up a high local electric field that leads to a soft breakdown in the SiO_x layer. As the resultant conduction and resistive switching are intrinsic properties of SiO_x, they can be induced in the SiO_x by different molecules or other exogenous materials atop the SiO_x substrate.[15] This SiO_x soft breakdown-induced conduction and resistive switching might be the cause of various qualitatively similar electrical behaviors in molecule layers,[4,5] carbon materials,[8−11] nanowires,[12,13] and bare nanogaps,[26−28] in which little attention, if any, was formerly paid to the SiO_x substrates.

Besides building up high local fields, the initial conduction from molecules or nanomaterials also provides current local heating, which could assist the electroforming in SiO_x because thermal annealing was found to introduce more defects at the SiO_x surface.[14,16] These introduced defects could serve as electron hopping centers so that electroforming is more easily induced at a voltage below the hard-breakdown threshold. This is also the case for the bare polySi−SiO_x−polySi structures (Figure 1c) in which thermal annealing (600 °C, 10 min, Ar/H_2 = 150/50 sccm) prior to electrical characterizations was adopted to facilitate the electroforming process. With a layer of APTES molecules, which introduce both enhanced local electric field and current local heating, the system can be readily electroformed as described in Figure 1a without thermal annealing. Not surprisingly, coating the bare polySi−SiO_x−polySi structure with a thin layer (5 nm) of amorphous carbon can serve the same role and leads to the electroforming of SiO_x and similar nonlinear electrical behavior[8,9] (see Supporting Information Figure S2). Note that while electrical breakdown in bulk SiO_x usually requires an electric field larger than 10 MV/cm, a SiO_x surface in contact with other exogenous nanomaterials, or that is subjected to thermal annealing, has more defects and is therefore an easier material in which to induce soft breakdown at a lower electric field. Consequently, the conduction in the vertical polySi−SiO_x−polySi is found to be localized at the vertical SiO_x edge.[14]

While the appearance of a current peak requires a voltage sweep above V_{max}, current hysteresis can be readily produced in the set region with $V > V_{th}$ (see V_{th} definition in Figure 2b). For example, starting from an OFF state, any voltage sweep to a value above V_{th} incurs the set process and thus current hysteresis. The conductance increase in the hysteretic loop can be abrupt (top panel in Figure 6a) or gradual featuring multistage set processes (bottom panel in Figure 6a). These behaviors can not only mimic current hysteresis in molecular systems,[29] but also in mechanical switches where similar vertical M−SiO_x−M stacking structures were adopted.[30,31] As V_{set} is smaller than V_{reset}, this type of hysteresis is always unidirectional (counter-clockwise) toward a higher-conductance state. The nonvolatility also determines that the same hysteresis is not reproducible before a reset operation is performed. In particular, a reset operation cannot be performed by sweeping to the opposite polarity of $-|V_{set}|$ (Figure 6b), but needs to sweep further to $-|V_{reset}|$. This features the typical unipolar resistive switching that is only voltage-magnitude dependent but not polarity dependent. It should be noted that some resistive-switching systems[32,33] were presented similarly in both polarities, but these are essentially unipolar behaviors as described in Figure 4b.

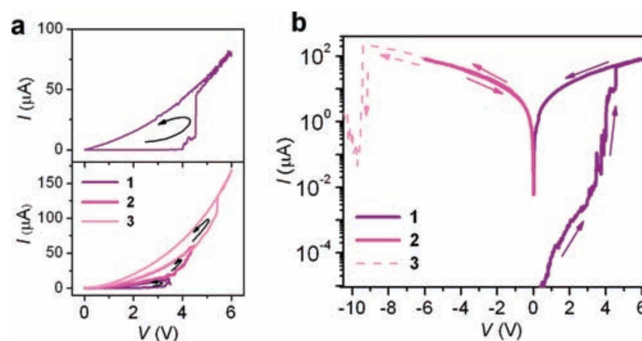

Figure 6. (a) Top panel: A hysteretic *IV* curve featuring a set operation in a vertical polySi−SiO_x−polySi device with 40 nm SiO_x. Bottom panel: Multiple hysteretic *IV* curves featuring a series of multistage set operations in a vertical polySi−SiO_x−polySi device with 10 nm SiO_x. The arrows indicate the sweep directions, and the numbers indicate the sweep orders. (b). *IV* sweeps in both polarities in a polySi−SiO_x−polySi device with 40 nm SiO_x. Curve 1 shows a set process (0 V → +6 V → 0 V) in the positive bias region. Curve 2 shows a subsequent voltage sweep (0 V → −6 V → 0 V) in the negative bias region, with no reset operation incurred. Curve 3 shows the next voltage sweep (0 V → −12 V) that triggers a reset operation at ∼ −9 V.

The underlying cause for all the above electrical phenomena is voltage-driven formation and modification of conduction filaments (Si−NC pathways) embedded in the SiO_x matrix. A certain minimum voltage is required to electrochemically modify the conducting pathway. Generally, the current peak appears at $|V_{max}| > 3$ V, which indicates that resistive-switching behavior below 3 V is unlikely from SiO_x. However, there is no clear maximum V_{max}, because interface resistance can reduce the actual voltage drop across the SiO_x, thus pushing V_{max} above 10 V.[15] The *IV* curve in the "read" region ($V < V_{th}$) is comparatively smooth and dominated by tunneling. Above V_{th}, as voltage-driven modifications of the conducting filaments begin, current fluctuations begin. These fluctuations alone produce various local current peaks (e.g., see Figure 6), which are not reproducible. They also persist in the electroforming process prior to the formation of a resistive-switching state (Supporting Information Figure S1). Therefore, careful attention should be paid to molecular and nanosystem characterizations, in which the reproducibility of the *IV* curves is sometimes not described or is neglected. The resistive switching in SiO_x needs to be in an oxygen-deficient environment and cannot be performed in ambient environment.[14] This may be due to the Si-filamentary nature where current local heating-induced oxidation prevents the conductance modulation. However, once "programmed" by electroforming, the resistance states are air-stable with a retention time projected to be above years.[14,22] This can be a good point of difference from some charge-based molecular memory systems in which the states decay faster.[7,32,34]

2. NDR and Current Hysteresis at Low Voltage (<3 V). Although the mechanisms for the resistive switching and related nonlinear conduction in various molecular and nanomaterial systems are largely unknown and debatable,[35] many have turned out to be through localized filamentary conduction.[35−37] In this form, the resistance change can be generally viewed as the result of electronic structural change by doping or electrochemical reactions[35] in the conducting pathways. Therefore, the conductance can be modulated in a nonvolatile manner. Meanwhile, the energy gaps between the highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO) can produce NDR behavior through resonant tunneling,[38−40] an effect similar to that in a resonant tunneling diode. Because resonant tunneling results from energy-level alignment between the electrodes and the molecular orbitals modulated by an external bias, the conductance change is volatile. Also, as tunneling current decays exponentially with molecular dimensions, resonant tunneling is usually observed in monolayer or few-layer molecules at low voltage bias (<3 V) with limited currents.[41,42] These aspects differ from the resistive-switching related nonlinear behaviors in the SiO_x discussed above.

Nevertheless, we find that at a post soft-breakdown state, SiO_x can also show similar resonant tunneling at a low voltage region (Figure 7a), with the current-peak location and current level close to those observed in molecular systems.[41,42] The appearance of this behavior can be understood based on a mechanistic picture of conduction through an aligned Si−NC pathway.[14] During the process of electroforming, or at an OFF state, the discontinuity of the Si−NCs gives rise to the possibility of forming an isolated Si−NC island along the pathway (Figure 7b). The confinement in the Si−NC island results in discrete energy levels, thus the resonant tunneling effect. This proposed mechanistic picture is indeed supported by the experimental observation of NDR in a Si quantum dot array.[43] Because a read voltage (e.g., <3 V) is not expected to induce structural change in the filament, the *IV* curve is reproducible (Figure 7a). The gradual degradation of the NDR upon continuous voltage sweeps (Figure 7a), which was also observed in molecules,[44] may be due to charge-trap effects. As the morphology of the filament can be altered during electroforming or after different programming processes, variations in this resonant-like NDR are expected, even in the same device at different stages of the filament evolution. This is shown in the inset in Figure 7a; three different NDR curves from the same SiO_x device can be obtained after different reset processes. The appearance of this resonant-like NDR behavior in SiO_x is comparatively low (within 5% in different OFF states), while the remainder are through typical tunneling as described before (Figure 2b). It should be noted that, due to the semianalogue conductance modulation through multistage set (Figure 6a) or reset processes (Figure 2c) described above, various resistance states ranging from kΩ to GΩ can be achieved in SiO_x. These conductions, although perhaps without NDR, can still mimic nonohmic conduction in molecules.[2,3]

SiO_x can also produce other effects in the low voltage region. Figure 7c shows an *IV* curve with an abrupt conductance jump at ∼0.65 V and, when tracking back, a sudden conductance drop at ∼0.5 V, producing a hysteresis window of ∼0.15 V. Similar electrical behavior has also been observed in single molecules.[45] The actual cause for this behavior in SiO_x needs further investigation. It is likely that some sudden trapping and detrapping events happen upon certain threshold voltages, thus rapidly modulating the conductance.

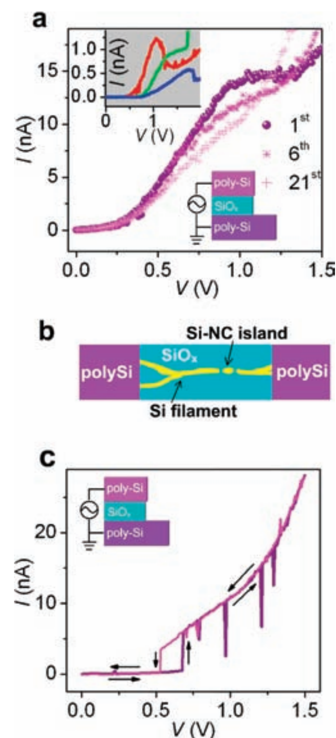

Figure 7. (a) NDR at low voltage in a polySi−SiO_x−polySi device (illustrated in the bottom inset) having the same structure and parameters as described in Figure 1c. The numbers indicate the numbers of voltage sweeps, showing a gradual disappearance of the NDR by the 21st sweep. Top inset shows three different NDR curves obtained in a similar device at different OFF states programmed by reset processes. (b) A schematic showing an isolated Si−NC island in the filamentary path. (c) Current hysteresis at low voltage (0 V → 1.5 V → 0 V) in a polySi−SiO_x−polySi device (illustrated in the top inset) having the same structure and parameters as described in Figure 1c. The arrows indicate the voltage-sweep directions.

Finally, we tested a native-oxide layer (1.5−3 nm) atop a conducting polySi surface. Unlike previous systems where the SiO_x layers are intentionally grown, here the SiO_x layer is naturally formed on the Si surface in an ambient environment. This is relevant to some Si-electrode-based molecular systems[46,47] in which, although SiO_x may be not intentionally used, a native-oxide layer will inevitably be produced when the electrodes are fabricated.[40,44,48] We tested the electrical property of this native-oxide layer by directly landing two probe tips (tip diameters are ∼20 um) on the polySi surface (see illustration in inset of Figure 8a). We first formed a good ohmic contact between one tip and the polySi surface by a voltage sweep to a high value (e.g., >5 V) to induce a hard electrical breakdown in the native-oxide layer. We then landed the other tip to a new location. Hence, the electrical phenomena come from one tip−SiO_x−polySi interface. Figure 8a shows a series of hysteretic *IV* loops from one of the interfaces we tested. Here, the hysteresis differs from a set process in the resistive-switching curves (Figure 6a) in that after each sweep loop, the subsequent sweep still starts with an OFF state, featuring the reproducibility and volatile property. The observed phenomena are very similar to those hysteretic behaviors observed in molecular systems at low voltage.[49,50] In addition to clear conductance-increase steps in Figure 8a, Figure 8b shows another series of current hysteretic *IV* curves with large current fluctuations from a native-oxide interface. Note that in both electrical phenomena, the native-oxide layer has not yet experienced a hard electrical

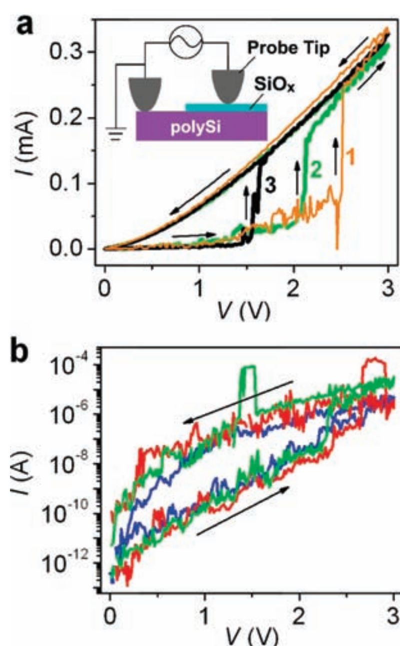

Figure 8. Electrical phenomena from surface native oxide. (a) Hysteretic *IV* curves from a surface native-oxide layer (1.5−3 nm thick). The numbers indicate the voltage-sweep order, and the arrows indicate the voltage-sweep direction. The inset is a schematic of the electrical setup. (b) Another series of hysteretic *IV* curves from a surface native-oxide layer, with the arrows indicting the voltage-sweep direction.

breakdown, which is indicated from the reproducibility of the hysteresis and low conductance. Hence, the phenomena are likely to be charge-trap related. Hard electrical breakdown in the native-oxide layer is induced at a voltage above 3 V, after which the interface is permanently in an ohmic-contact state with no hysteretic behavior. For this reason, resistive switching and related nonlinear behavior as described before (Figure 2) are not observed in native-oxide layers.

CONCLUSION

We have demonstrated various electrical phenomena including resistive switching and related nonlinear electrical behaviors, current hysteresis, and NDR intrinsic to a thin layer of SiO_x. These behaviors can largely mimic various electrical phenomena observed in molecules and other nanomaterials. The underlying cause for these effects is voltage-driven and high-electric-field-induced soft breakdown in the SiO_x layer. In particular, this soft breakdown can be readily induced by unintended factors, such as defects in a SiO_x surface, material-assisted local electric-field enhancement, and current local heating as described in this Article. Many other studies have been conducted in detailing the physical mechanism of SiO_x breakdown and conduction.[51] Our study and results call for care when investigating conduction in electronic systems with SiO_x as a nominally passive component. The forming processes, behaviors, and mechanisms have been discussed in detail, providing a potential guide to distinguish electrical phenomena in molecules and nanomaterials of interest from those in SiO_x.

ASSOCIATED CONTENT

Supporting Information. Material preparation details; Figure S1 showing electroforming processes in vertical poly-Si−SiO_x−polySi; and Figure S2 showing resistive-switching *IV* curves in an amorphous-carbon-coated vertical polySi−SiO_x−polySi device. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Author
lzhong@rice.edu; natelson@rice.edu; tour@rice.edu

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